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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/848,778
Filing Date: May 03, 2001
Appellant(s): BEEREL ET AL.

Scott C. Harris
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/27/2006 appealing from the Office action mailed 06/29/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,933,462	VITERBI et al.	8-1999

F. Thomson Leighton, Introduction to Parallel Algorithms and Architectures: Arrays-Trees-Hypercubes, Morgan Kaufmann Publishers, Inc., 1992, pages 1-3, 36-45, 238 and 239

S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, Soft-Output Decoding Algorithms in Iterative Decoding of Turbo Codes, TDA progress Report 42-124~ Feb. 15, 1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

1. Claims 1, 2, 6-12, 15-17, 19, 36-38, 42-47, 50-52, 61-63, 67-71, 74-76, 85-90, 93, 94, 97, 98, 101 and 102 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viterbi; Andrew J. et al. (US 5933462 A, hereafter referred to as Viterbi) in view of Thomson Leighton (F. Thomson Leighton, Introduction to Parallel Algorithms and

Architectures: Arrays-Trees-Hypercubes, Morgan Kaufmann Publishers, Inc., 1992, pages 1-3, 36-45, 238 and 239).

35 U.S.C. 103(a) rejection of claims 1, 8, 9, 12, 16 and 17.

Viterbi teaches demodulating the received encoded signal to produce soft information (See Figure 1 and 3 in Viterbi); and iteratively processing the soft information with one or more soft-in/soft-output SISO modules (Figure 4 in Viterbi is a decoder having a feedback loop for iteratively processing soft information according to the iterative algorithm of Figure 7 in Viterbi; col. 3, lines 66-67 and col. 4, lines 66-67 in Viterbi teach clearly suggest the intent to replace to replace the MAP decoders typically used in a turbo decoder with SOVA decoders; Note: a SOVA decoder is inherently a decoder accepting soft inputs to perform Viterbi's algorithm to produce soft outputs; hence a SOVA decoder **is also a SISO decoder**; the Examiner suggests the Hagenauer treatise included in the Examiner's PTO-892 for teachings on SOVA decoders), at least one SISO module using a tree structure arranged to perform prefix and suffix operations to compute forward and backward state metrics (the Forward Viterbi Decoder 24 in Figure 4 of Viterbi teaches a first SISO module using the Trellis tree structure of Figure 5 to perform prefix operations to compute forward state metrics $I_k(s)$ in Equation 5 in col. 6 of Viterbi and the Backward Viterbi Decoder 24 in Figure 4 of Viterbi teaches a second SISO module using the Trellis tree structure of Figure 5 to perform suffix operations to compute backward state metrics $\vartheta_{k-1}(s')$ in Equation 6 in col. 6 of Viterbi; Note: the Appellant defines prefix operations recursively as $z_0=y_0$ and $z_i= y_0 \otimes \ldots \otimes y_i$, it is easy to

see that Equation 5 in col. 6 of Viterbi is a prefix operation by letting $z_0=y_0=I_0$, k=i and z_i $=I_i(s)y_i(s',s)$ when $\otimes$ is multiplication, likewise equation 6 of Viterbi satisfies suffix operations if the suffix operations are defined as on page 21 of the Appellant's disclosure).

Viterbi teaches receiving an input signal corresponding to output from one or more block encoding modules (col. 7, lines 40-44 in Viterbi teach one or more block encoding modules; Note: turbo encoders and SCIC codes are comprised of one or more block encoding modules). Note: one of ordinary skill in the art at the time the invention was made would have recognized that the algorithm in Viterbi is a computationally intensive algorithm.

However Viterbi does not explicitly teach the specific use of **parallel** prefix and suffix operations [Emphasis Added].

Thomson Leighton, in an analogous art, teaches use of **parallel** prefix and suffix operations (Figure 1-21 on page 38 of Thomson Leighton teaches the use of parallel prefix computations for prefix operations or computations such as the forward prefix operations or computations taught in Viterbi; problem 1.27 on page 239 of Thomson Leighton teaches the obvious extension of prefix operations to suffix operations). One of ordinary skill in the art at the time the invention was made would have been highly motivated to combine Viterbi with Thomson Leighton recognizing that the computations in Viterbi are computationally intensive and the parallel prefix and suffix computations in Thomson Leighton provide a parallel algorithm used for computationally intensive algorithms to speed processing up (see top line of page 2 in Thomson Leighton).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Viterbi with the teachings of Thomson Leighton by including use of **parallel** prefix and suffix operations. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of **parallel** prefix and suffix operations would have provided a parallel algorithm used for computationally intensive algorithms to speed processing up (see top line of page 2 in Thomson Leighton).

35 U.S.C. 103(a) rejection of claims 36, 37, 44-47, 51, 52, 61-62, 69-71, 75, 76, 85-90, 93, 94, 97, 98, 101 and 102.

Viterbi teaches demodulating the received encoded signal to produce soft information (See Figure 1 and 3 in Viterbi); and iteratively processing the soft information with one or more soft-in/soft-output SISO modules (Figure 4 in Viterbi is a decoder having a feedback loop for iteratively processing soft information according to the iterative algorithm of Figure 7 in Viterbi; col. 3, lines 66-67 and col. 4, lines 66-67 in Viterbi teach clearly suggest the intent to replace to replace the MAP decoders typically used in a turbo decoder with SOVA decoders; Note: a SOVA decoder is inherently a decoder accepting soft inputs to perform Viterbi's algorithm to produce soft outputs; hence a SOVA decoder **is also a SISO decoder**; the Examiner suggests the Hagenauer treatise included in the Examiner's PTO-892 for teachings on SOVA decoders), at least one SISO module using a tree structure arranged to perform prefix and suffix operations to

compute forward and backward state metrics (the Forward Viterbi Decoder 24 in Figure 4 of Viterbi teaches a first SISO module using the Trellis tree structure of Figure 5 to perform prefix operations to compute forward state metrics $I_k(s)$ in Equation 5 in col. 6 of Viterbi and the Backward Viterbi Decoder 24 in Figure 4 of Viterbi teaches a second SISO module using the Trellis tree structure of Figure 5 to perform suffix operations to compute backward state metrics $\vartheta_{k-1}(s')$ in Equation 6 in col. 6 of Viterbi; Note: the Appellant defines prefix operations recursively as $z_0=y_0$ and $z_i= y_0 \otimes \ldots \otimes y_i$, it is easy to see that Equation 5 in col. 6 of Viterbi is a prefix operation by letting $z_0=y_0=I_0$, k=i and $z_i =I_i(s)y_i(s',s)$ when $\otimes$ is multiplication, likewise equation 6 of Viterbi satisfies suffix operations if the suffix operations are defined as on page 21 of the Appellant's disclosure).

In addition, Viterbi teaches receiving an input signal corresponding to one or more outputs of a finite state machine (A convolutional encoder is inherently an FSM hence the received input signal corresponds to one or more outputs of a finite state machine: Note: a Trellis is also an FSM for the convolutional code). The Examiner asserts the a decoder performs the inverse operations to an encoder for the purposes of recovering the original signal prior to encoding, hence; the decoder of Figure 4 in Viterbi determines the soft decoded inverse of the originally encoded soft output since the decoder is soft output (SOVA) decoder.

Viterbi teaches receiving an input signal corresponding to output from one or more block encoding modules (col. 7, lines 40-44 in Viterbi teach one or more block encoding modules; Note: turbo encoders and SCIC codes are comprised of one or more block encoding modules). Note: one of ordinary skill in the art at the time the invention was made would have recognized that the algorithm in Viterbi is a computationally intensive algorithm.

However Viterbi does not explicitly teach the specific use of **parallel** prefix and suffix operations [Emphasis Added].

Thomson Leighton, in an analogous art, teaches use of **parallel** prefix and suffix operations (Figure 1-21 on page 38 of Thomson Leighton teaches the use of parallel prefix computations for prefix operations or computations such as the forward prefix operations or computations taught in Viterbi; problem 1.27 on page 239 of Thomson Leighton teaches the obvious extension of prefix operations to suffix operations). One of ordinary skill in the art at the time the invention was made would have been highly motivated to combine Viterbi with Thomson Leighton recognizing that the computations in Viterbi are computationally intensive and the parallel prefix and suffix computations in Thomson Leighton provide a parallel algorithm used for computationally intensive algorithms to speed processing up (see top line of page 2 in Thomson Leighton). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Viterbi with the teachings of Thomson Leighton by including use of **parallel** prefix and suffix operations. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made,

because one of ordinary skill in the art would have recognized that use of **parallel** prefix and suffix operations would have provided a parallel algorithm used for computationally intensive algorithms to speed processing up (see top line of page 2 in Thomson Leighton).

35 U.S.C. 103(a) rejection of claims 2, 6, 7, 19, 38, 42, 43, 63, 67 and 68.

Page 6, line 5 of the Appellant's specification marginalization-combining operations-as is any pair of operations that satisfy the commutative semi-ring properties. Multiplication and addition over field elements used in the calculation of forward state metrics $I_k(s)$ in Equation 5 in col. 6 of Viterbi backward state metrics $\vartheta_{k-1}(s')$ in Equation 6 in col. 6 of Viterbi are marginalization-combining operations since the Multiplication and addition are over a field and any field is a semi-ring.

35 U.S.C. 103(a) rejection of claims 10.

Note: claim 10 is an intended use claim. The Examiner asserts that the decoding devices in Viterbi are communication devices; hence using the decoding devices taught in Viterbi is an obvious embodiment of the teachings in Viterbi since that is what the decoder is designed for and do not require any structural changes in the decoder taught in the Viterbi patent. See Ex parte Masham, 2 USPQ2d 1647 (1987).

35 U.S.C. 103(a) rejection of claims 11.

See blocks 74 and 78 in Figure 7 of Viterbi.

35 U.S.C. 103(a) rejection of claims 15, 50, 59 and 74.

Note: a Brent-Kung tree is a specific obvious embodiment of a Trellis tree structure.

2. Claims 3-5, 13, 14, 18, 39-41, 48, 49, 53-60, 64-66, 72, 73, 77-84, 91, 92, 95, 96, 99 and 100 are rejected under 35 U.S.C. 103(a) as being unpatentable over Viterbi; Andrew J. et al. (US 5933462 A, hereafter referred to as Viterbi) and Thomson Leighton (F. Thomson Leighton, Introduction to Parallel Algorithms and Architectures: Arrays-Trees-Hypercubes, Morgan Kaufmann Publishers, Inc., 1992, pages 1-3, 36-45, 238 and 239) in view of Benedetto et al. (S. Benedetto, D. Divsalar, G. Montorsi, and F. Pollara, Soft-Output Decoding Algorithms in Iterative Decoding of Turbo Codes, TDA progress Report 42-124, Feb. 15, 1996).

35 U.S.C. 103(a) rejection of claims 3, 4, 39, 40, 64 and 65.

Viterbi and Thomson Leighton, substantially teaches the claimed invention described in claims 1, 2, 6-12, 15-17, 19, 36-38, 42-47, 50-52, 61-63, 67-71, 74-76, 85-90, 93, 94, 97, 98, 101 and 102 (as rejected above).

However Viterbi and Thomson Leighton, does not explicitly teach the specific use of Min-sum operations.

Pages 72-73 of Benedetto, in an analogous art, teach max-sum operations. The Examiner asserts that since 1/x is a minimum if x is a maximum so that use of min-sum

operations is an obvious embodiment of the teachings in Benedetto, since the operations are inherently equivalent.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings Viterbi and Thomson Leighton with those of Benedetto by including use of Min-sum operations. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of Min-sum operations would have provided the opportunity to to reduce the complexity for computing forward and backward metrics since multiplication and addition operations are exchanged for maximum and addition operations (see top of page 73 in Benedetto).

35 U.S.C. 103(a) rejection of claims 5, 41 and 66.

See equation 21 on page 72 of Benedetto.

35 U.S.C. 103(a) rejection of claims 13, 48 and 72.

Figure 6 on page 79 of Benedetto teaches using soft output of a first SISO as soft input to another SISO.

35 U.S.C. 103(a) rejection of claims 14, 49 and 73.

The max-sum operations at the top of page 73 in Benedetto for backward and forward metrics are recursive with a latency of $O(\log_2 N)$.

35 U.S.C. 103(a) rejection of claims 18, 53 and 77.

The log-BCJR algorithm taught in Benedetto starting on page 71 is a sliding-window algorithm implemented by tiling an observation interval into subintervals called windows; and applying a minimum half-window SISO operation on each subinterval of the window.

35 U.S.C. 103(a) rejection of claim 54, 55, 57, 60, 78, 79, 81, 84, 91, 92, 95, 96, 99 and 100.

Viterbi teaches demodulating the received encoded signal to produce soft information (See Figure 1 and 3 in Viterbi); and iteratively processing the soft information with one or more soft-in/soft-output SISO modules (Figure 4 in Viterbi is a decoder having a feedback loop for iteratively processing soft information according to the iterative algorithm of Figure 7 in Viterbi; col. 3, lines 66-67 and col. 4, lines 66-67 in Viterbi teach clearly suggest the intent to replace to replace the MAP decoders typically used in a turbo decoder with SOVA decoders; Note: a SOVA decoder is inherently a decoder accepting soft inputs to perform Viterbi's algorithm to produce soft outputs; hence a SOVA decoder **is also a SISO decoder**; the Examiner suggests the Hagenauer treatise included in the Examiner's PTO-892 for teachings on SOVA decoders), at least one SISO module using a tree structure arranged to perform parallel prefix and suffix operations to compute forward and backward state metrics (the Forward Viterbi Decoder 24 in Figure 4 of Viterbi teaches a first SISO module using the Trellis tree structure of Figure 5 to perform parallel prefix operations to compute forward state

metrics $I_k(s)$ in Equation 5 in col. 6 of Viterbi and the Backward Viterbi Decoder 24 in Figure 4 of Viterbi teaches a second SISO module using the Trellis tree structure of Figure 5 to perform parallel suffix operations to compute backward state metrics $\vartheta_{k-1}(s')$ in Equation 6 in col. 6 of Viterbi; Note: the Appellant defines prefix operations recursively as $z_0=y_0$ and $z_i= y_0 \otimes \ldots \otimes y_i$, it is easy to see that Equation 5 in col. 6 of Viterbi is a prefix operation by letting $z_0=y_0=I_0$, k=i and $z_i =I_i(s)y_i(s',s)$ when $\otimes$ is multiplication, likewise equation 6 of Viterbi satisfies suffix operations if the suffix operations are defined as on page 21 of the Appellant's disclosure).

In addition Viterbi teaches receiving an input signal corresponding to one or more outputs of a finite state machine (A convolutional encoder is inherently an FSM hence the received input signal corresponds to one or more outputs of a finite state machine: Note: a Trellis is also an FSM for the convolutional code).

Viterbi teaches receiving an input signal corresponding to output from one or more block encoding modules (col. 7, lines 40-44 in Viterbi teach one or more block encoding modules; Note: turbo encoders and SCIC codes are comprised of one or more block encoding modules). Note: one of ordinary skill in the art at the time the invention was made would have recognized that the algorithm in Viterbi is a computationally intensive algorithm.

However Viterbi does not explicitly teach the specific use of **parallel** prefix and suffix operations [Emphasis Added].

Thomson Leighton, in an analogous art, teaches use of **parallel** prefix and suffix operations (Figure 1-21 on page 38 of Thomson Leighton teaches the use of parallel prefix computations for prefix operations or computations such as the forward prefix operations or computations taught in Viterbi; problem 1.27 on page 239 of Thomson Leighton teaches the obvious extension of prefix operations to suffix operations). One of ordinary skill in the art at the time the invention was made would have been highly motivated to combine Viterbi with Thomson Leighton recognizing that the computations in Viterbi are computationally intensive and the parallel prefix and suffix computations in Thomson Leighton provide a parallel algorithm used for computationally intensive algorithms to speed processing up (see top line of page 2 in Thomson Leighton). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Viterbi with the teachings of Thomson Leighton by including use of **parallel** prefix and suffix operations. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of **parallel** prefix and suffix operations would have provided a parallel algorithm used for computationally intensive algorithms to speed processing up (see top line of page 2 in Thomson Leighton).

However Viterbi and Thomson Leighton does not explicitly teach the specific use of a demodulator adapted to receive as input a signal encoded by a finite state machine (FSM) and to produce soft information relating to the received signal.

Benedetto, in an analogous art, teaches the Soft Demodulator of Figure 2 on page 66 of Benedetto receives an encoded signal and demodulates the received encoded signal to produce soft information; Note: convolutional or the turbo code taught in the Benedetto paper is produced using sequential logic, i.e., an FSM.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Viterbi and Thomson Leighton with the teachings of Benedetto by including use of a demodulator adapted to receive as input a signal encoded by a finite state machine (FSM) and to produce soft information relating to the received signal. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a demodulator adapted to receive as input a signal encoded by a finite state machine (FSM) and to produce soft information relating to the received signal would have provided the opportunity to provide required soft information to the soft decoders in the Viterbi patent (Note: a SOVA decoder is inherently a decoder accepting soft inputs to perform Viterbi's algorithm to produce soft outputs; hence a SOVA decoder **is also a SISO decoder**; the Examiner suggest the Hagenauer treatise included in the Examiner's PTO-892 for teachings on SOVA decoders).

35 U.S.C. 103(a) rejection of claims 56 and 80.

Figure 6 on page 79 of Benedetto teaches using soft output of a first SISO as soft input to another SISO.

35 U.S.C. 103(a) rejection of claims 58 and 82.

The max-sum operations at the top of page 73 in Benedetto for backward and forward metrics are recursive with a latency of $O(\log_2 N)$.

35 U.S.C. 102(e) rejection of claims 59 and 83.

Note: a Brent-Kung tree is a specific obvious embodiment of a Trellis tree structure.

(10) Response to Argument

Summary of rejection:

Viterbi teaches maximum-likelihood decoding using backward and forward state metric calculations over a Trellis (a tree structure as in Figure 2 and 5 of Viterbi). Forward state metric operations are prefix operations and backward state metric operations are suffix operations (see rejection of claim 1, above), which the Appellant agrees with (Appellant's response, page 3, 04/12/2006). In particular, if the word "parallel" were removed from in front of the phrase "prefix and suffix operations" in claim 1, then Viterbi would teach each and every element of claim 1 (see rejection of claim 1, above), which the Appellant does not dispute. The Examiner would like to point out that algorithms for "prefix and suffix operations" have been developed independently in error correction and computational mathematics/computer science, whereby practitioners in error correction refer to "prefix and suffix operations" as backward and forward state metric calculations and practitioners in computational mathematics/computer use the term "prefix and suffix operations" as is.

Leighton teaches parallel "prefix and suffix operations" (see rejection of claim 1, above). Leighton is combined with Viterbi so that together, Leighton combined with Viterbi teach each and every element of claim 1 (see rejection of claim 1, above), which the Appellant does not dispute.

The Examiner provides the motivation for combining, which comes from Leighton (see rejection of claim 1, above): a desire to speed up processing, which the Appellant disputes. The Appellant claims that the motivation is based on hindsight not found in Leighton. In response to appellant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, the Examiner disagrees and asserts that it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the Appellant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

The Examiner asserts conversion of traditional serial algorithms to parallel algorithms for the purpose of speeding up computations is not the Appellant's invention and precedes even the Leighton book, although, Leighton explicitly and clearly teaches the conversion of traditional serial algorithms to parallel algorithms for the purposes of a speed up (last paragraph page 7 to first paragraph page 8 in Leighton). In fact, parallel processing is the art of optimally converting traditional serial algorithms to parallel algorithms and, although, Leighton teaches some of the parallel algorithms that have

been converted from traditional serial algorithms, the parallel algorithms and the motivation to use the algorithms, in Leighton, precedes Leighton.

The Appellant did not invent prefix and suffix computations, which precede the Viterbi patent and is explicitly taught in the Viterbi patent.

The Appellant did not invent **parallel** prefix and suffix operations, which precede the Leighton reference and are explicitly taught in the Leighton reference.

The Appellant did not invent the motivation for parallel processing –a speed up in computations-, which precedes the Leighton reference, is explicitly taught in the Leighton reference and is the sole motivation for the existence of the Leighton reference (Note: the Leighton reference presents parallel algorithms for the express purpose of reformulating various serial algorithms into parallel algorithms for speeding up computations, last paragraph page 7 to first paragraph page 8 in Leighton).

Below the Examiner responds to each and every one of the Appellant's arguments:

Pages 7 and 8 of the Appellant's Appeal Brief summarize the Appellant's view of the Appellant's invention.

On page 9, lines 1-6 of the Appellant's Appeal brief, the Appellant contends, the motivation for combining "to speed processing up" comes from hindsight.

In response to appellant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, the Examiner disagrees and asserts that it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the Appellant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

The Examiner asserts conversion of traditional serial algorithms to parallel algorithms for the purpose of speeding up computations is not the Appellant's invention and precedes even the Leighton book, although, Leighton explicitly and clearly teaches the conversion of traditional serial algorithms to parallel algorithms for the purposes of a speed up (last paragraph page 7 to first paragraph page 8 in Leighton). In fact, parallel processing is the art of optimally converting traditional serial algorithms to parallel algorithms and, although, Leighton teaches some of the parallel algorithms that have been converted from traditional serial algorithms, the parallel algorithms and the motivation to use the algorithms, in Leighton, precedes Leighton.

On page 10, paragraph 1 to line 11, page 11 of the Appellant's Appeal brief, the Appellant contends, "If Viterbi et al. were modified to use parallel computation, it would expressly contradict the teaching of Viterbi et al. and specifically the teaching of reducing memory consumption. If Viterbi et al. were modified to use parallel processing,

it would no longer reduce the memory consumption in the way suggested by Viterbi et al".

The Examiner disagrees and asserts that SISO is a generic term used for constituent decoders for a turbo decoder. Currently two types of decoders are used for the constituent SISO decoders in a turbo decoder: Soft-Output Viterbi Algorithm (SOVA) decoders and MAP decoders (col. 3, lines 51-65 in Viterbi). SOVA decoders are less complex and easier to implement than MAP decoders, which are more efficient than SOVA decoders. Col. 4 lines 1-15 in Viterbi teach that using a SOVA decoder in place of a MAP decoder also reduces memory requirements since MAP decoders are memory intensive. The Examiner asserts that Leighton teaches that using **parallel** prefix and suffix operations in a SOVA decoder would also provide a desirable speed up (last paragraph page 7 to first paragraph page 8 in Leighton). There is nothing in the Viterbi patent that remotely teaches away from the Leighton patent since parallel prefix and suffix operations in the Leighton apply to the prefix and suffix operations for the SOVA decoder in Equations 5 and 6 in column 6 of Viterbi and not the MAP decoder that the Viterbi patent refers to in column 4, lines 1-6 of Viterbi.

On page 11, lines 8-11 of the Appellant's Appeal brief, the Appellant contends, "The hypothetical combination of Viterbi et al. in view of the Thomson Leighton reference would be an improper combination, since it would require contradicting the teaching of Viterbi et al".

The Examiner disagrees and asserts that Viterbi teaches the advantages of using the Soft-Output **Viterbi** Algorithm (SOVA) over the MAP algorithm for obvious reasons. The Appellant's assertion would only be true, if parallel prefix and suffix operations were not compatible with Viterbi's algorithm and forced the use of the MAP algorithm. Since parallel prefix and suffix operations in the Leighton apply to the prefix and suffix operations for the SOVA decoder in Equations 5 and 6 in column 6 of Viterbi, qan algorithm using parallel prefix and suffix operations is entirely compatible with the Soft-Output **Viterbi** Algorithm (SOVA) and provides the benefit of a speed-up in computations.

The last paragraph on page 11 continuing on to page 12 of the Appellant's Appeal brief continue to present arguments regarding hindsight, which the Examiner has fully addressed, above.

On page 12, last paragraph of the Appellant's Appeal brief, the Appellant contends, "In addition, Appellants would like to take issue with the statement in the Official Action that "there is a multitude of prior art teaching various algorithms for using the prefix and suffix computations"". At this point, it is the Examiner's opinion that the current arts are sufficient for a Prima facie case, as pointed out, above. If the Appeal board disagrees, the Appeal board will provide a detailed discussion on why. Based on the Appeal boards decision, the Examiner will determine the best way to proceed and will make a determination of what additional Prior Arts are relevant.

Paragraph 1 on page 13 to paragraph 1 in the Appellant's Appeal brief summarize the Appellants previous arguments. The Examiner summarizes the Examiner's arguments, again, below:

The Examiner asserts conversion of traditional serial algorithms to parallel algorithms for the purpose of speeding up computations is not the Appellant's invention and precedes even the Leighton book, although, Leighton explicitly and clearly teaches the conversion of traditional serial algorithms to parallel algorithms for the purposes of a speed up (last paragraph page 7 to first paragraph page 8 in Leighton). In fact, parallel processing is the art of optimally converting traditional serial algorithms to parallel algorithms and, although, Leighton teaches some of the parallel algorithms that have been converted from traditional serial algorithms, the parallel algorithms and the motivation to use the algorithms, in Leighton, precedes Leighton.

In summary, the Appellant did not invent prefix and suffix computations, which precede the Viterbi patent and is explicitly taught in the Viterbi patent.

The Appellant did not invent **parallel** prefix and suffix operations, which precede the Leighton reference and are explicitly taught in the Leighton reference.

The Appellant did not invent the motivation for parallel processing –a speed up in computations-, which precedes the Leighton reference, is explicitly taught in the Leighton reference and is the sole motivation for the existence of the Leighton reference (Note: the Leighton reference presents parallel algorithms for the express purpose of

reformulating various serial algorithms into parallel algorithms for speeding up computations, last paragraph page 7 to first paragraph page 8 in Leighton).

On page 14, paragraph 2 of the Appellant's Appeal brief, the Appellant contends, "the official action states that one having ordinary skill in the art "only has to recognize" that forward state metrics are prefix operations. With all due respect, this recognition, made by the Official Action, is made only with the benefit of the present specification". The Examiner would like to point out that, forward state metric operations are prefix operations and backward state metric operations are suffix operations (see rejection of claim 1, above), which the Appellant agrees with (Appellant's response, page 3, 04/12/2006). The Examiner asserts that even if the Appellant were the first to discover that forward state metric operations are prefix operations and backward state metric operations are suffix operations, a discovery is not an invention. Viterbi et al. discovered the use of prefix and suffix operations for decoding convolution codes. Parallel prefix and suffix operations predate Leighton and are designed for use with any application such as the one in the Viterbi using Prefix and suffix computations (Last paragraph, page 42 Leighton).

On page 15, lines 1-14 of the Appellant's Appeal brief are purely speculative in an attempt to invent reasons hindering the combination and not taught in the Viterbi patent, for example, Viterbi does not a last-in-first out buffer among other things. Such contention requires evidence, citing figures, lines and columns where such elements are

taught, just as the Appellant requires of the Examiner for presenting a Prima Facie case.

The last paragraph on page 15 to the first paragraph of page 17 of the Appellant's Appeal brief argues that data dependencies would prohibit the combination. The Appellant's arguments are purely speculative. Viterbi only teaches that the prefix and suffix operations (Equations 5 and 6 in column 6 of Viterbi) are required. Viterbi does not teach any data dependencies associated with the calculations of the prefix and suffix operations in Equations 5 and 6 in column 6. In Fact, nowhere in the Viterbi patent does Viterbi make any suggestion of how to calculate the prefix and suffix operations in Equations 5 and 6 in column 6. As such, the Appellant's contentions on page 15 to the first paragraph of page 17 of the Appellant's Appeal brief are purely speculative without foundation. For such a contention to hold, the Appellant needs to cite real evidence: citing figures, lines and columns where such elements are taught, just as the Appellant requires of the Examiner for presenting a Prima Facie case.

The last paragraph on page 17 to the first paragraph of page 18 of the Appellant's Appeal brief summarize the Appellant's previous arguments.

On page 18, paragraph 2 of the Appellant's Appeal brief, the Appellant basically argues the same elements as above, contending that in addition to the previously argued elements of claim 1, the Prior art does not teach the limitation "determining a soft

inverse of the finite state machine" in claim 36. Note also, that claim 36 recites, "using a tree structure arranged to perform parallel prefix and suffix operations" not --using a tree structure arranged to perform parallel prefix and suffix **architecture**--.

The Examiner disagrees and asserts that Viterbi teaches receiving an input signal corresponding to one or more outputs of a finite state machine (A convolutional encoder is inherently an FSM hence the received input signal corresponds to one or more outputs of a finite state machine: Note: a Trellis is also an FSM for the convolutional code). The Examiner asserts the a decoder performs the inverse operations to an encoder for the purposes of recovering the original signal prior to encoding, hence; the decoder of Figure 4 in Viterbi determines the soft decoded inverse of the originally encoded soft output since the decoder is soft output (SOVA) decoder.

On page 18, paragraph 3 of the Appellant's Appeal brief, the Appellant argues the same elements as above for claim 54. Note also, that claim 54 recites, "using a tree structure arranged to perform parallel prefix and suffix operations" not --using a tree structure arranged to perform parallel prefix and suffix **architecture**--.

On page 18, paragraph 2 of the Appellant's Appeal brief, the Appellant basically argues the same elements as above, contending that in addition to the previously argued elements of claim 1, the Prior art does not teach the limitation "determining a soft inverse" in claim 61. Note also, that claim 61 recites, "using a tree structure arranged to

perform parallel prefix and suffix operations" not --using a tree structure arranged to perform parallel prefix and suffix **architecture**--.

The Examiner asserts the a decoder performs the inverse operations to an encoder for the purposes of recovering the original signal prior to encoding, hence; the decoder of Figure 4 in Viterbi determines the soft decoded inverse of the originally encoded soft output since the decoder is soft output (SOVA) decoder.

The first paragraph on page 19 to the second paragraph of page 20 of the Appellant's Appeal brief present the same arguments as above, which have all been addressed, above.

Section 2 on page 20 of the Appellant's Appeal brief presents no new arguments.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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